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AUTHOR(S):

Fujiwara, H; Kimoto, T; Tojo, T; Matsunami, H

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# Characterization of in-grown stacking faults in 4H–SiC (0001) epitaxial layers and its impacts on high-voltage Schottky barrier diodes

H. Fujiwara<sup>a)</sup>

*Department of Electronic Science and Engineering, Kyoto University, Kyotodaigaku-katsura, Nishikyo, Kyoto 615-8510, Japan and Department Technical and Development, Toyotanso, 2181-2 Ohnohara Mitoyo, Kagawa 769-1612, Japan*

T. Kimoto

*Department of Electronic Science and Engineering, Kyoto University, Kyotodaigaku-katsura, Nishikyo, Kyoto 615-8510, Japan*

T. Tojo

*Department Technical and Development, Toyotanso, 2181-2 Ohnohara Mitoyo, Kagawa 769-1612, Japan*

H. Matsunami

*Department of Electronic Science and Engineering, Kyoto University, Kyotodaigaku-katsura, Nishikyo, Kyoto 615-8510, Japan*

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The density, shape and structure of in-grown stacking faults in 4H–SiC (0001) epitaxial layers have been characterized by cathodeluminescence, photoluminescence and high-resolution transmission electron microscopy. These analyses indicate that in-grown stacking faults are of 8H structure, and are generated mostly near the epilayer/substrate interface during chemical vapor deposition. The impact of the stacking faults on the performance of 4H–SiC (0001) Schottky barrier diodes has been investigated. It is revealed that the stacking faults cause the lowering of Schottky barrier height as well as the decrease of breakdown voltage. © 2005 American Institute of Physics.

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Superior properties of silicon carbide (SiC) make this material an attractive candidate for fabricating power devices with high breakdown voltage and lower power loss. In spite of rapid progress in SiC crystal growth techniques, there still exist several kinds of structural defects such as micropipes, screw dislocations, basal plane dislocations and stacking faults in SiC epilayers. Thick 4H–SiC epilayers with a significantly reduced defect density are required for high-power devices.

It is widely recognized that micropipes significantly deteriorate the breakdown voltage and cause increasing leakage current in SiC power devices.<sup>1</sup> Although the reduction of micropipes has been extensively studied in both bulk<sup>2</sup> and epitaxial growth,<sup>3</sup> the density of screw/edge dislocations in SiC is still high. Screw dislocations in SiC *pn* diodes lead to the onset of microplasma at slightly lower reverse voltage than theoretical breakdown voltage.<sup>4</sup> The influence of screw dislocations and other defects on breakdown voltage of Schottky barrier diodes has been also investigated.<sup>5–9</sup> On the other hand, it is reported that triangular defects cause the deterioration of reverse characteristics of *P-i-n* diodes.<sup>10</sup> Transmission electron microscopy (TEM) analysis revealed that at least one stacking fault (SF) exists in the triangular defect.<sup>11</sup> Although Kojima *et al.* reported that stacking faults (SFs) severely affect the reverse characteristics of 4H–SiC (11 $\bar{2}$ 0) Schottky barrier diodes,<sup>12</sup> it is not clear how stacking faults affect the device performance on the off-axis (0001) Si face. In this letter, the authors describe the characterization of in-grown stacking faults in thick 4H–SiC (0001) epilayers

and investigate impacts of stacking faults on the characteristics of Schottky barrier diodes.

Epitaxial growth was carried out with a vertical hot-wall chimney-type chemical vapor deposition (CVD) reactor in a SiH<sub>4</sub>–C<sub>3</sub>H<sub>8</sub>–H<sub>2</sub> system at a growth temperature of 1835 °C.<sup>13</sup> Thick (52–53  $\mu$ m) epilayers were grown with a growth rate of 34  $\mu$ m/h on 8° off-axis 4H–SiC (0001) substrates. Stacking faults were detected by panchromatic cathodeluminescence (CL) at room temperature. The nature and structure of stacking faults were characterized by photoluminescence (PL) and cross-sectional transmission electron microscopy (TEM). Ni Schottky barrier diodes with and without stacking faults were fabricated on the thick epilayers with a donor concentration of  $2\text{--}5 \times 10^{14}$  cm<sup>–3</sup>. The diameter of Ni Schottky contacts was 300  $\mu$ m. The forward and reverse current-voltage characteristics were evaluated at 200, 290, and 373 K.

Figure 1 shows the panchromatic CL image obtained from a 52- $\mu$ m-thick epilayer at room temperature. Although most stacking faults are hardly detected in optical microscopy, a clear feature is seen in CL images: Each triangular feature in Fig. 1 corresponds to one stacking fault. The stacking fault density depends on the initial process of CVD growth. For example, by sufficient removal of subsurface damage of substrates, the stacking fault density can be reduced to about 0–1 cm<sup>–2</sup>. Powell and co-workers have reported that removal of subsurface damage prior to CVD is essential for homoepitaxial growth of high-quality hexagonal SiC polytypes.<sup>14,15</sup> In CL images, radiative recombination is dominated by a broad peak at 465 nm (2.67 eV) from stacking faults. The stacking faults are composed of the edges along [11 $\bar{2}$ 0], [1 $\bar{1}$ 00] and either [10 $\bar{1}$ 0] or [01 $\bar{1}$ 0] as a right-

<sup>a)</sup> Author to whom correspondence should be addressed; electronic mail: h.fujiwara@toyotanso.co.jp

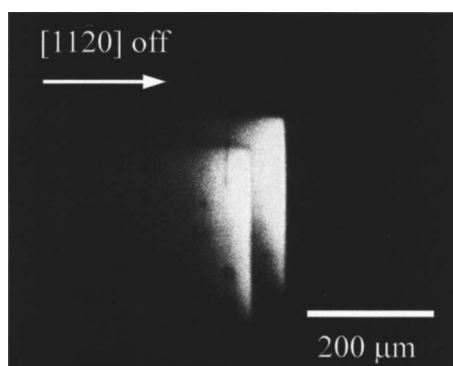


FIG. 1. Panchromatic CL image at room temperature taken from a 52- $\mu$ m-thick 4H-SiC epilayer with stacking faults.

angle triangle, or  $[1\bar{1}00]$ ,  $[10\bar{1}0]$  and  $[01\bar{1}0]$  as an isosceles triangle. The total length of stacking faults along the  $[11\bar{2}0]$  off direction was estimated from the stacking fault size along  $[1\bar{1}00]$  (perpendicular to the off direction) and the angle of triangle shape ( $30^\circ$  or  $60^\circ$ ). Then, the depth of stacking fault generation point was calculated from the total length and off angle ( $8^\circ$ ). This analysis revealed that most ( $>75\%$ ) stacking faults are generated near the epilayer/substrate interface, indicating that these defects are in-grown stacking faults.

Figure 2 shows a cross-sectional high-resolution transmission electron microscopy image taken from a stacking fault location of 52- $\mu$ m-thick epilayer, zone axis of which is  $[2\bar{1}\bar{1}0]$ . It is observed that the 4H-SiC stacking sequence (22222...) is replaced by a peculiar sequence (224422...). Thus, the stacking fault is of 4H/8H/4H structure. Although only two stacking faults were analyzed by TEM in this study, both stacking faults were of 8H structure. Izumi *et al.* also reported that the 8H structure is dominant in in-grown stacking faults in 4H-SiC grown by CVD.<sup>16</sup> Thus the 8H structure may be a rather common stacking fault in epitaxially grown 4H-SiC.

In PL measurements at 18 K, a weak and broad peak in the range from 2.56 to 2.70 eV is observed in only the epilayers including stacking faults. PL peaks due to phonon replicas of free exciton recombination in several polytype inclusions have been reported.<sup>16,17</sup> In PL measurements of 4H-SiC epilayers which contain 8H stacking faults, peaks at 2.62–2.68 eV were observed,<sup>16</sup> which also agrees with the present study. In the forward bias degradation of SiC *P-i-n* diodes, several studies have been made on the structure and formation mechanism of stacking faults. It has been suggested that the stacking faults consist of two partial disloca-

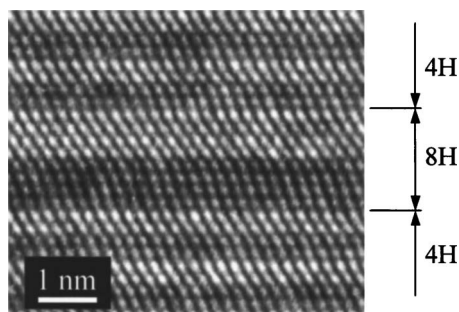


FIG. 2. Cross-sectional high-resolution TEM image of an in-grown stacking fault in a 4H-SiC epilayer.

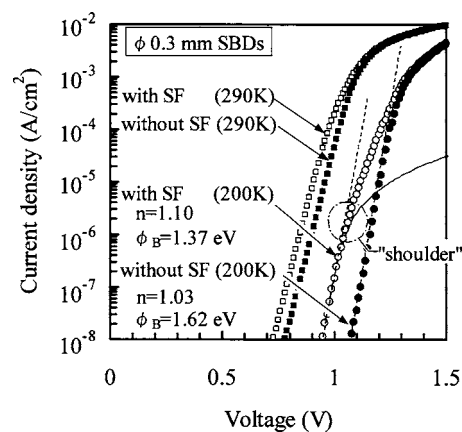


FIG. 3. Typical forward characteristics of Ni Schottky barrier diodes with and without stacking faults on 52- $\mu$ m-thick 4H-SiC epilayers.

tions with Burgers vectors of  $1/3[10\bar{1}0]$  and  $1/3[01\bar{1}0]$ , which nucleate from a perfect dislocation with a Burgers vector of  $1/3[11\bar{2}0]$ .<sup>18</sup> Most stacking faults in stressed *P-i-n* diodes show a triangular shape with edges along  $[1\bar{1}00]$ ,  $[2\bar{1}\bar{1}0]$  and  $[\bar{1}2\bar{1}0]$  with an angle of  $120^\circ$ . The structure of stacking faults in such diodes has been identified as mostly single-layer stacking faults.<sup>19</sup> The peak related to the stacking faults has been observed at 2.88–2.98 eV in electroluminescence and CL.<sup>20</sup> Therefore the in-grown stacking faults observed in this study are different in both structure and optical property from the stacking faults in degraded *P-i-n* diodes. The formation mechanism of stacking faults is, however, not clear at present.

Figure 3 represents the typical forward characteristics of Ni Schottky barrier diodes with and without stacking faults, but no other visible surface defects. Diodes without stacking faults exhibit a small ideality factor of 1.01–1.05, and the Schottky barrier height was determined to be 1.62–1.66 eV. The current-voltage characteristics of Schottky barrier diodes with stacking faults at 290 K are shifted toward the low voltage region, suggesting the existence of “low-barrier-height” region.<sup>8,9</sup> This expectation was confirmed in the current-voltage characteristics at 200 K, as shown in Fig. 3, where a clear shoulder appeared in the low voltage ( $\sim 1.0$  V) region. From this shoulder characteristic, the Schottky barrier height for low-barrier-height region could be estimated to be 1.37 eV, about 0.25 eV lower than the normal value. The authors speculate that this lowered Schottky barrier height might be correlated with stacking faults, which appear on the surface of off-axis (0001) epilayers.

The reverse characteristics of 60 Schottky barrier diodes with and without stacking faults were measured. In the leakage current measurements at an elevated temperature of 373 K, however, almost all Schottky barrier diodes showed low leakage current (close to a noise level:  $10^{-8}$ – $10^{-9}$  A/cm<sup>2</sup> at  $-1000$  V), and the influences of stacking faults were not clear. Assuming that the Schottky barrier heights of diodes with and without stacking faults are 1.37 and 1.62 eV, respectively, the theoretical leakage current was calculated from a thermionic field emission model.<sup>21</sup> The leakage current theoretically expected was estimated to be as low as the  $10^{-13}$  A/cm<sup>2</sup> range even for diodes including stacking faults, because of the relatively high barrier height of Ni and still AIP license or copyright, see <http://apl.aip.org/apl/copyright.jsp>

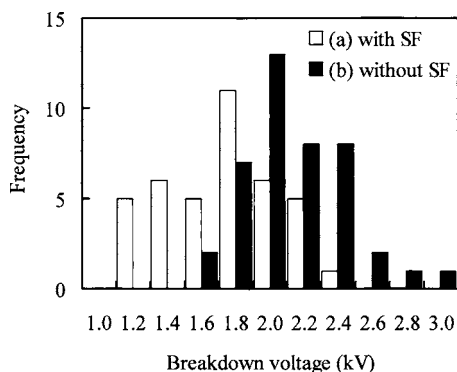


FIG. 4. Breakdown voltage of Ni Schottky barrier diodes (a) with and (b) without stacking faults on 52- $\mu\text{m}$ -thick 4H-SiC epilayers (donor concentration:  $2\text{--}5 \times 10^{14} \text{ cm}^{-3}$ ).

low electric field (0.44 MV/cm) at  $-1000 \text{ V}$ . This may be the reason why the impacts of stacking faults on leakage current were not significant, at least up to  $-1000 \text{ V}$ . The breakdown voltage of 80 Schottky barrier diodes with and without stacking faults was also measured at room temperature. The diodes that contain stacking faults exhibited reduced (approximately 20% lower) breakdown voltage as shown in Fig. 4. The average (maximum) breakdown voltage of diodes with and without stacking faults was 1800 V (2400 V) and 2200 V (3050 V), respectively. Furthermore, the Schottky barrier diodes with stacking faults tended to show much higher leakage current near breakdown. This soft breakdown behavior could be seen in the diodes with stacking faults, probably due to the enhanced tunneling current through the low-barrier-height region at high electric field, while the diodes without stacking faults showed hard breakdown. The number of stacking faults existing in Schottky contact area was varied from zero to five in this study. The existence of stacking faults itself was critical, and the variation of stacking fault number (1–5) in Schottky barrier diodes showed very minor effects on the reverse characteristics.

In summary, structure, optical properties, and impacts on diodes characteristics of in-grown stacking faults in thick 4H-SiC (0001) epilayers have been investigated. The in-grown stacking faults have the 8H structure, and exhibited PL peaks at 2.56–2.70 eV. The stacking faults influenced the

current-voltage characteristics of Schottky barrier diodes, especially Schottky barrier height and breakdown voltage. The Schottky barrier diodes that contain stacking faults exhibited approximately 20% lower breakdown voltage.

- <sup>1</sup>P. G. Neudeck and J. A. Powell, *IEEE Electron Device Lett.* **15**, 63 (1994).
- <sup>2</sup>D. Nakamura, I. Gunjishima, S. Yamaguchi, T. Ito, A. Okamoto, H. Kondo, S. Onda, and K. Takatori, *Nature (London)* **430**, 1009 (2004).
- <sup>3</sup>I. Kamata, H. Tsuchida, T. Jikimoto, and K. Izumi, *Jpn. J. Appl. Phys., Part 2* **41**, L1137 (2002).
- <sup>4</sup>P. G. Neudeck, W. Huang, and M. Dudley, *IEEE Trans. Electron Devices* **46**, 478 (1999).
- <sup>5</sup>D. T. Morissette and J. A. Cooper, Jr., *Mater. Sci. Forum* **389–393**, 1133 (2002).
- <sup>6</sup>Q. Wahab, A. Ellison, A. Henry, C. Hallin, J. D. Persio, R. Martinez, and E. Janzén, *Appl. Phys. Lett.* **76**, 2725 (2000).
- <sup>7</sup>T. Tsuji, S. Izumi, A. Ueda, H. Fujisawa, K. Ueno, H. Tsuchida, I. Kamata, T. Jikimoto, and K. Izumi, *Mater. Sci. Forum* **389–393**, 1141 (2002).
- <sup>8</sup>D. Defives, O. Noblanc, C. Dua, C. Brylinski, M. Barthula, V. Aubry-Fortuna, and F. Meyer, *IEEE Trans. Electron Devices* **46**, 449 (1999).
- <sup>9</sup>H. Saitoh, T. Kimoto, and H. Matsunami, *Mater. Sci. Forum* **457–460**, 997 (2004).
- <sup>10</sup>T. Kimoto, N. Miyamoto, and H. Matsunami, *IEEE Trans. Electron Devices* **46**, 471 (1999).
- <sup>11</sup>T. Okada, T. Kimoto, K. Yamai, H. Matsunami, and F. Inoko, *Mater. Sci. Eng., A* **361**, 67 (2003).
- <sup>12</sup>K. Kojima, T. Ohno, T. Fujimoto, M. Katsuno, N. Ohtani, J. Nishio, Y. Ishida, T. Takahashi, T. Suzuki, T. Tanaka, and K. Arai, *Appl. Phys. Lett.* **81**, 2974 (2002).
- <sup>13</sup>K. Fujihira, T. Kimoto, and H. Matsunami, *J. Cryst. Growth* **255**, 136 (2003).
- <sup>14</sup>J. A. Powell, J. B. Petit, J. H. Edgar, I. G. Jenkins, L. G. Matus, J. W. Yang, P. Pirouz, W. J. Choyke, L. Clemen, and M. Yoganathan, *Appl. Phys. Lett.* **59**, 333 (1991).
- <sup>15</sup>P. G. Neudeck and J. A. Powell, *Silicon Carbide, Recent Major Advances*, edited by W. J. Choyke, H. Matsunami, and G. Pensl (Springer, Berlin, 2003), pp. 9 and 179.
- <sup>16</sup>S. Izumi, H. Tsuchida, T. Tawara, I. Kamata, and K. Izumi, *Mater. Sci. Forum* **483–485**, 323 (2005).
- <sup>17</sup>S. Bai, G. Wagner, E. Shishkin, W. J. Choyke, R. P. Devaty, M. Zhang, P. Pirouz, and T. Kimoto, *Mater. Sci. Forum* **389–393**, 589 (2002).
- <sup>18</sup>H. Jacobson, J. P. Bergman, C. Hallin, E. Janzén, T. Tuomi, and H. Lendenmann, *J. Appl. Phys.* **95**, 1485 (2004).
- <sup>19</sup>J. Q. Liu, M. Skowronski, C. Hallin, R. Söderholm, and H. Lendenmann, *Appl. Phys. Lett.* **80**, 749 (2002).
- <sup>20</sup>S. G. Sridhara, F. H. C. Carlsson, J. P. Bergman, and E. Janzén, *Appl. Phys. Lett.* **79**, 3944 (2001).
- <sup>21</sup>T. Hatakeyama, M. Kushibe, T. Watanabe, S. Imai, and T. Shinohe, *Mater. Sci. Forum* **433–436**, 831 (2003).